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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:
Kriz et al.

MMB Docket No. **1890-0038**

Application No. **10/757,360**

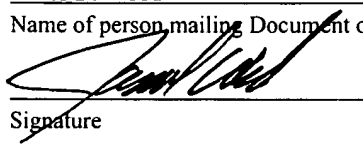
Filed: **January 13, 2004**

For: **Method for Manufacturing a Bipolar Transistor Having a Polysilicon Emitter**

Examiner: **To be assigned**

Group Art Unit: **2812**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on
July 20, 2004
(Date of deposit)
James D. Wood
Name of person mailing Document or fee



Signature

July 20, 2004
Date of Signature

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, Applicant hereby discloses the following references, copies of which are not enclosed, regarding the above-identified patent application.

Patent References

U.S. Patent No.	Inventor	Issue Date
6,319,786 B1	Gris	November 20, 2001
5,185,276	Chen et al.	February 9, 1993
5,204,276	Nakajima et al.	April 20, 1993
5,587,326	Takemura	December 24, 1996
5,001,533	Yamaguchi	March 19, 1991
2001/0005035 A1	Kinoshita	June 28, 2001
2001/0003667 A1	Ahn et al.	June 14, 2001

Foreign Application	Issue Date	Country
DE 3940674 A1	June 28, 1990	DE
DE 3304642A1	August 16, 1984	DE
FR 2795233 A1	June 18, 1999	FR
CA 01 201 218	February 25, 1986	CA

Articles

1) Pontcharra, de Jean, et al., "A 30-GHz f_T Quasi-Self-Aligned Single-Poly Bipolar Technology," IEEE Transactions on Electron Devices, New York US, November 1, 1997, Volume 44, No. 11, pages 2091 – 2096 (6 pages).
2) Sugiyama, M. et al., "A 40 GHz f_T Si Bipolar Transistor LSI Technology", Proceedings of the International Electron Devices Meeting, Washington, Dec. 3-6, 1989, New York US, December 3, 1989, pages 221 – 224, (4 pages).
3) Aoyama, T. et al., "Selective Polysilicon Deposition (SPD) by Hot-Wall LPCVD and its Application to High Speed Bipolar Devices", Japanese Journal of Applied Physics, Tokyo, Japan 1990, pages 665 – 668, (4 pages).
4) Burghartz J. N. et al., "Novel In-Situ Doped Polysilicon Emitter Process with Buried Diffusion Source (BDS)", IEEE Electron Device Letters, Volume 12, No. 12, New York US, December 1991, pages 679 – 681, (3 pages).
5) Selvakumar, C. R., "Theoretical and Experimental Aspects of Polysilicon Emitter Bipolar Transistors", IEEE, November 16, 1988, pages 3 – 16, (14 pages).

Documents U.S. 5,185,276, as well as the Articles, "A 30-GHz f_T Quasi-Self-Aligned Single-Poly Bipolar Technology", "A 40 GHz f_T Si Bipolar Transistor LSI Technology", and "Selective Polysilicon Deposition (SPD) by Hot-Wall LPCVD and Its Application to High Speed Bipolar Devices" were cited in a International Preliminary Examination Report (copy enclosed) in a related PCT patent application number PCT/EP02/08234 filed on July 10, 2002.

Documents U.S. 5,204,276, U.S. 5,587,326, U.S. 2001/0005035 A1, and U.S. 2001/0003667 A1 were cited in an International Search Report (copy enclosed) in a related PCT patent application number PCT/EP02/08234 filed on July 10, 2002.

Document "Theoretical and Experimental Aspects of Polysilicon Emitter Bipolar Transistors" was cited in the patent application U.S. Serial No. 10/757,360 filed January 13, 2004.

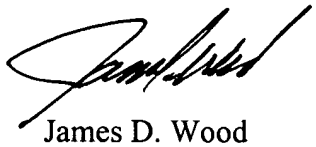
Documents DE 3940674 A1, DE 3304642A1, and FR 2795233 A1, as well as the articles "Novel In-Situ Doped Polysilicon Emitter Process with Buried Diffusion Source

(BDS)", "Selective Polysilicon Deposition (SPD) by Hot-Wall LPCVD and its Application to High Speed Bipolar Devices", "A 40 GHz f_T Si Bipolar Transistor LSI Technology", and "A 30-GHz f_T Quasi-Self-Aligned Single-Poly Bipolar Technology" were cited in an examination of the related German Patent Application 101, 34 089.3-33, filed on July 13, 2001.

U.S. 5,001,533 is an equivalent of DE 3940674 A1, CA 01 201 218 is an equivalent of DE 3304642A1, and U.S. 6,319,786 B1 is an equivalent of FR 2795233 A1.

It is believed that no fees are due for the consideration of this Information Disclosure Statement. However, the Commissioner is hereby authorized to charge any deficiency or to credit any overpayment to Deposit Account No. 13-0014, but not to include any payment of issue fees.

Respectfully Submitted,



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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	MMB DOCKET NO. 1890-0038	APPLICATION NO.: 10/757,360
	APPLICANT(S): Kriz et al.	
	FILING DATE: January 13, 2004	GROUP ART UNIT: 2812

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA	6,319,786 B1	November 20, 2001	Gris			
	AB	5,185,276	February 9, 1993	Chen et al.			
	AC	5,204,276	April 20, 1993	Nakajima et al.			
	AD	5,587,326	December 24, 1996	Takemura			
	AE	5,001,533	March 19, 1991	Yamaguchi			
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	AG	2001/0003667 A1	June 14, 2001.	Ahn et al.			
	AH						
	AI						
	AJ						
	AK						

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL	DE 3940674 A1	June 28, 1990	Germany			Yes No
	AM	DE 3304642 A1	August 16, 1984	Germany			Yes No
	AN	FR 2795233 A1	June 18, 1999	France			Yes No
	AO	CA 01 201 218	February 25, 1986	Canada			Yes No
	AP						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ	1	Pontcharra, de Jean, et al., "A 30-GHz f_T Quasi-Self-Aligned Single-Poly Bipolar Technology", IEEE Transactions on Electron Devices, New York US, November 1, 1997, Volume 44, No. 11, pages 2091 – 2906, (6 pages).
	AR	1	Sugiyama, M. et al., "A 40 GH f_T Si Bipolar Transistor LSI Technology", Proceedings of the International Electron Devices Meeting, Washington, Dec. 3-6, 1989, New York US, December 3, 1989, Pages 221 – 224, (4 pages)
	AS	1	Aoyama T. et al., "Selective Polysilicon Deposition (SPD) by Hot-Wall LPCVD and its Application to High Speed Bipolar Devices", Japanese Journal of Applied Physics, Tokyo, Japan 1990, pages 665 – 668, (4 pages).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicants.

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	MMB DOCKET NO. 1890-0038	APPLICATION NO.: 10/757,360
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	BA						
	BB						
	BC						
	BD						
	BE						
	BF						
	BG						
	BH						
	BI						
	BJ						
	BK						

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	BL						Yes No
	BM						Yes No
	BN						Yes No
	BO						Yes No
	BP						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AQ	2	Burghartz J. N. et al., "Novel In-Situ Doped Polysilicon Emitter Process with Buried Diffusion Source (BDS)", IEEE Electron Device Letters, Volume 12, No. 12, New York US, December 1991, pages 679 – 681, (3 pages).
	AR	2	Selvakumar, C. R., "Theoretical and Experimental Aspects of Polysilicon Emitter Bipolar Transistors", IEEE, November 16, 1988, pages 3 – 16, (14 pages).
	AS	2	

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